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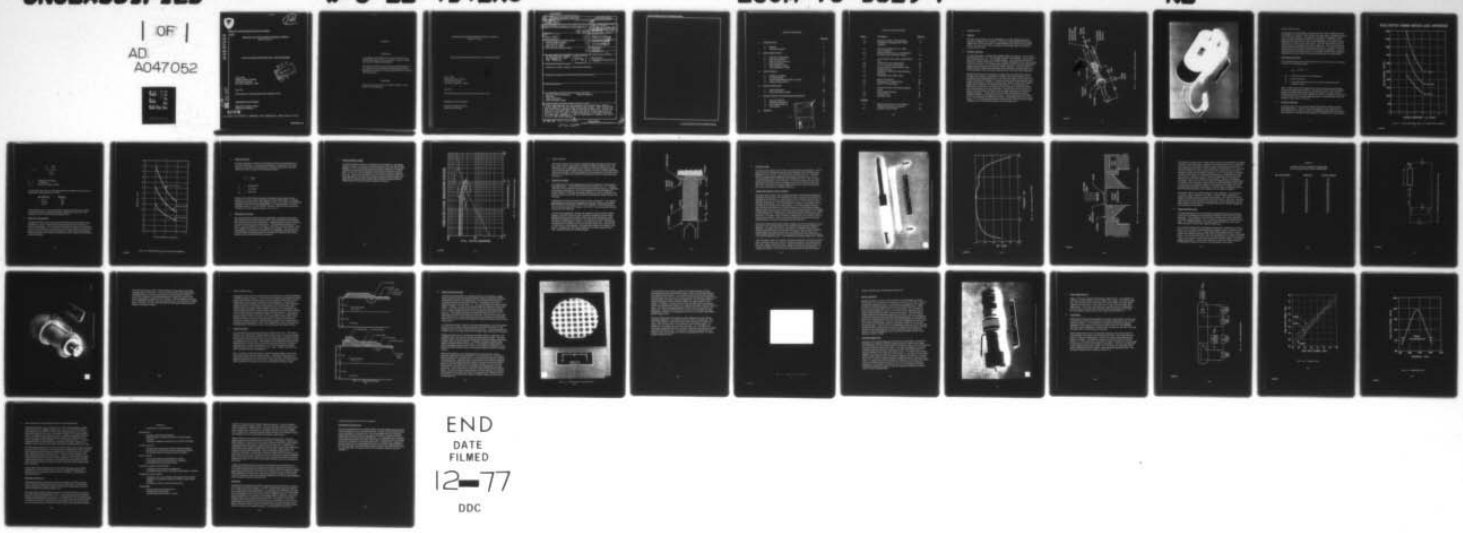

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Research and Development Technical Report

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RESEARCH AND DEVELOPMENT TECHNICAL REPORT
ECOM 75-1329 F

ELECTRON BEAM SEMICONDUCTOR L-BAND AMPLIFIER

B. W. Bell
Watkins-Johnson Company
3333 Hillview Avenue
Palo Alto, California 94304

July 1977

Final Report for Period 12 May 1975 to December 1976.

DISTRIBUTION STATEMENT

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EBS Diode
Diode processing
High peak power output

20. ABSTRACT *(Continue on reverse side if necessary and identify by block number)*

An EBS L-Band amplifier has been developed with characteristics making it ideally suited for IFF power amplification applications. These include high peak output power, high gain, high reliability and small size. Devices were tested at up to 1000 W peak at 1% duty and 1500 watts peak output power at 0.1% duty, with 23 dB gain, a 50 MHz bandwidth and a 50% target efficiency. The diode source impedance of 3 ohms is transformed by a quarter wave cavity up to a 50 ohm output impedance.

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1. INTRODUCTION

a. Objective

The goal of this program was the development of an EBS amplifier for use as the power amplifier in IFF systems. Performance goals included 2000 W peak output power, 25 dB power gain, 10 MHz bandwidth, and 60 percent overall efficiency. The device was to have an MTBF of 10,000 hours with a cost of $100 in quantities of 10,000.

b. Technical Approach

To meet these goals, a gridded EBS amplifier design was selected. This is shown schematically in Fig. 1-1. The essential elements of the amplifier are the electron gun, semiconductor target, and matching network. The triode-type electron gun produces a circular electron beam which is density modulated by an RF signal applied to the grid of the gun. The electron beam strikes the reverse-biased semiconductor target, producing electron-hole pairs by impact ionization. The diode output is matched into the required load impedance by the externally mounted quarter-wave cavity matching network and then transformed up to the 50 ohm output impedance.

During the first phase of the program a design study was conducted to optimize the diode area, geometry, epi thickness, doping, and source impedance to the particular device performance goals. This led to the design of a new diode mask set for fabrication of the diodes. During the next phase of the program the device design was completed, including the electron gun, input DC block, target holder/output window assembly, and output matching circuit. Sub-assemblies were fabricated and cold tests were performed where required to verify the performance characteristics of the sub-assemblies. When the diode mask set was completed, diode fabrication was begun; a total of eight diode runs were fabricated during the program. Testing of the devices continued through the program; seventeen devices were assembled and tested. One of these devices, WJ-3620 S/N 17, was packaged and delivered to ECOM. A photograph of the unit is shown in Fig. 1-2. The packaged unit includes the EBS device, the quarter-wave output matching cavity, and RFI filtering of all of the DC input leads.

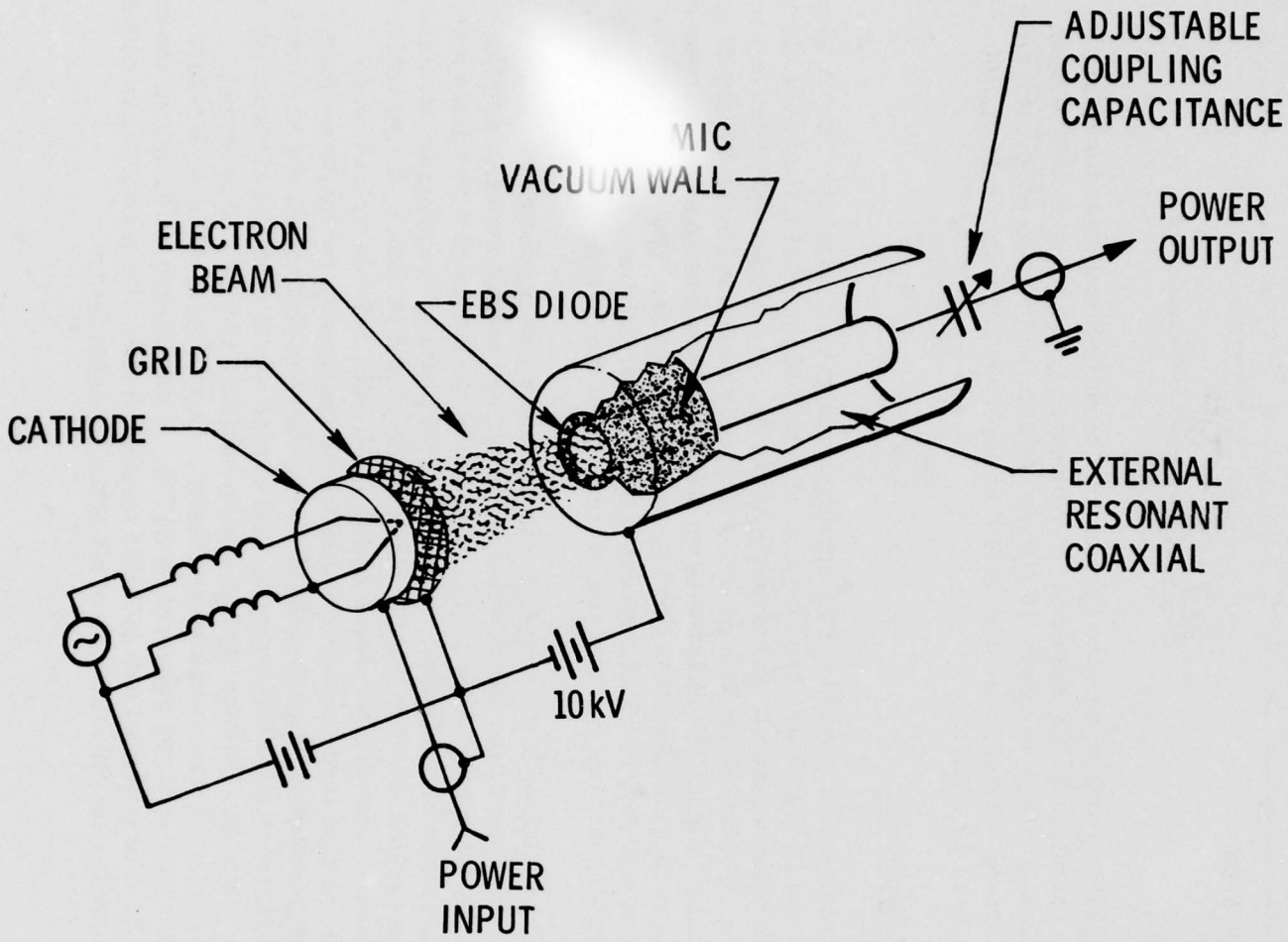

FIG. 1-1 - Schematic of EBS L-Band Amplifier

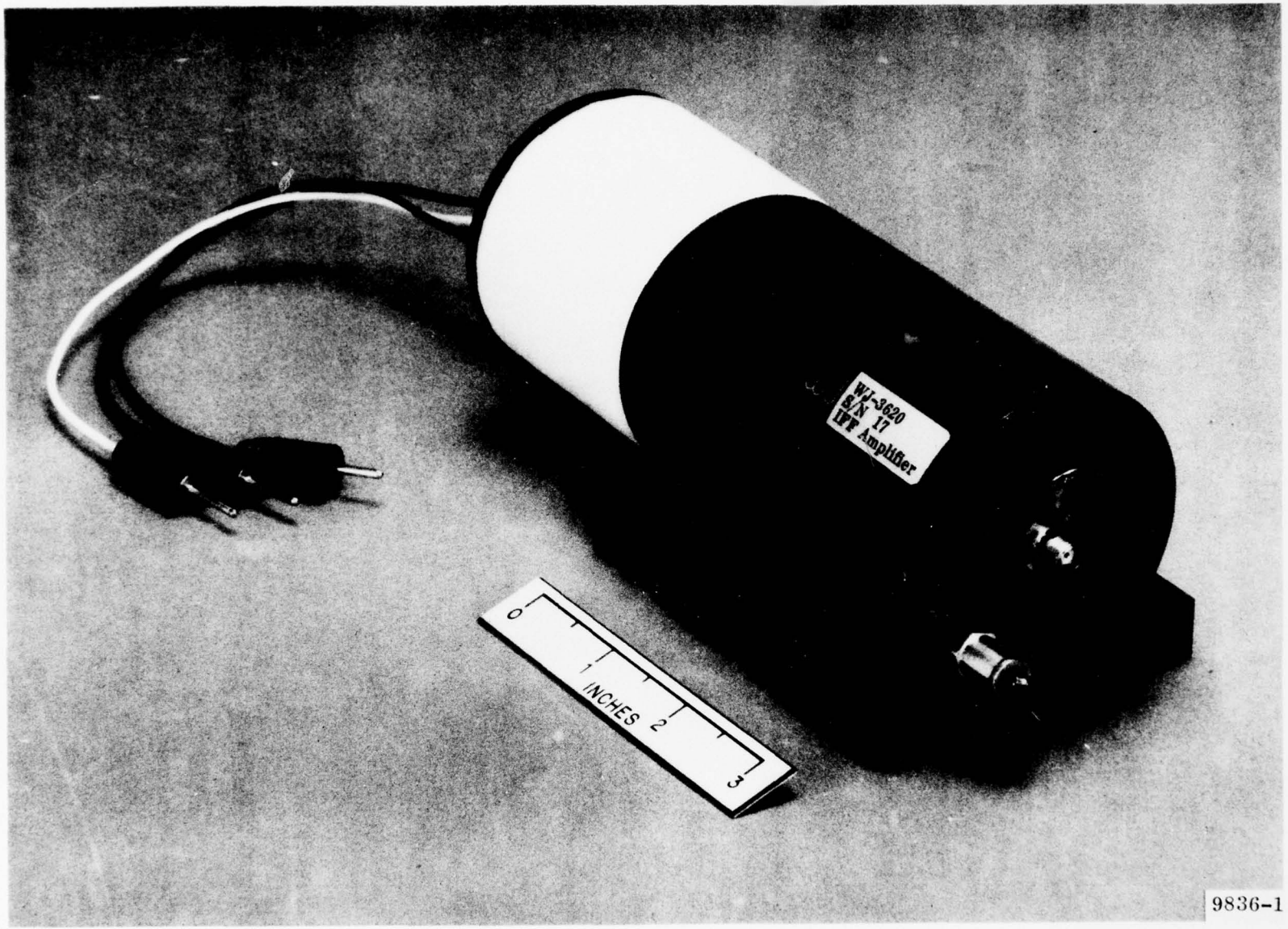

FIG. 1-2 - Photograph of packaged EBS L-Band Amplifier

2. DIODE DESIGN STUDY

The design of the semiconductor target for the EBS L-band amplifier involved the selection of a number of inter-related diode parameters, including the following: diode area, geometry, epi thickness, epi doping, metallization, capacitance, breakdown voltage, and diode source impedance. The diode source impedance was selected first, based on the capabilities of the output matching circuit and the required peak output power. The diode epi thickness was then selected based on the required transit time efficiency. These two parameters then determined the optimum epi doping and diode area. The diode breakdown voltage was then maximized, based on the epi doping and thickness. Based on these parameters, the diode mask set was designed, with the diode capacitance minimized by careful design of the guard ring and metal overlay geometries.

a. Diode Source Impedance

The relationship between the diode output power and the diode source impedance is given by the following equation:

$$P_{out} \quad (\Delta f)^2 R_b = K$$

Δf = Equivalent low-pass cut-off frequency

R_b = Source impedance

K = A constant determined by the peak electric field and electron velocity in silicon

Fig. 2-1 shows a plot of the output power versus the diode source impedance for several possible epi thicknesses. Working into the lower load impedances produces correspondingly greater output powers; however, losses are also increased and hence, the overall efficiency is reduced. Because of these losses in both the diode and the output matching circuit, a minimum diode source impedance of three ohms was selected.

b. Diode Epi Thickness

As shown in Fig. 2-1, increasing the diode epi thickness results in greater peak output powers. However, the device efficiency is also reduced due to transit-time losses in the epi region. The following equation gives the transit-time efficiency as a function of the frequency of operation and the epi thickness:

PEAK OUTPUT POWER VERSUS LOAD IMPEDANCE

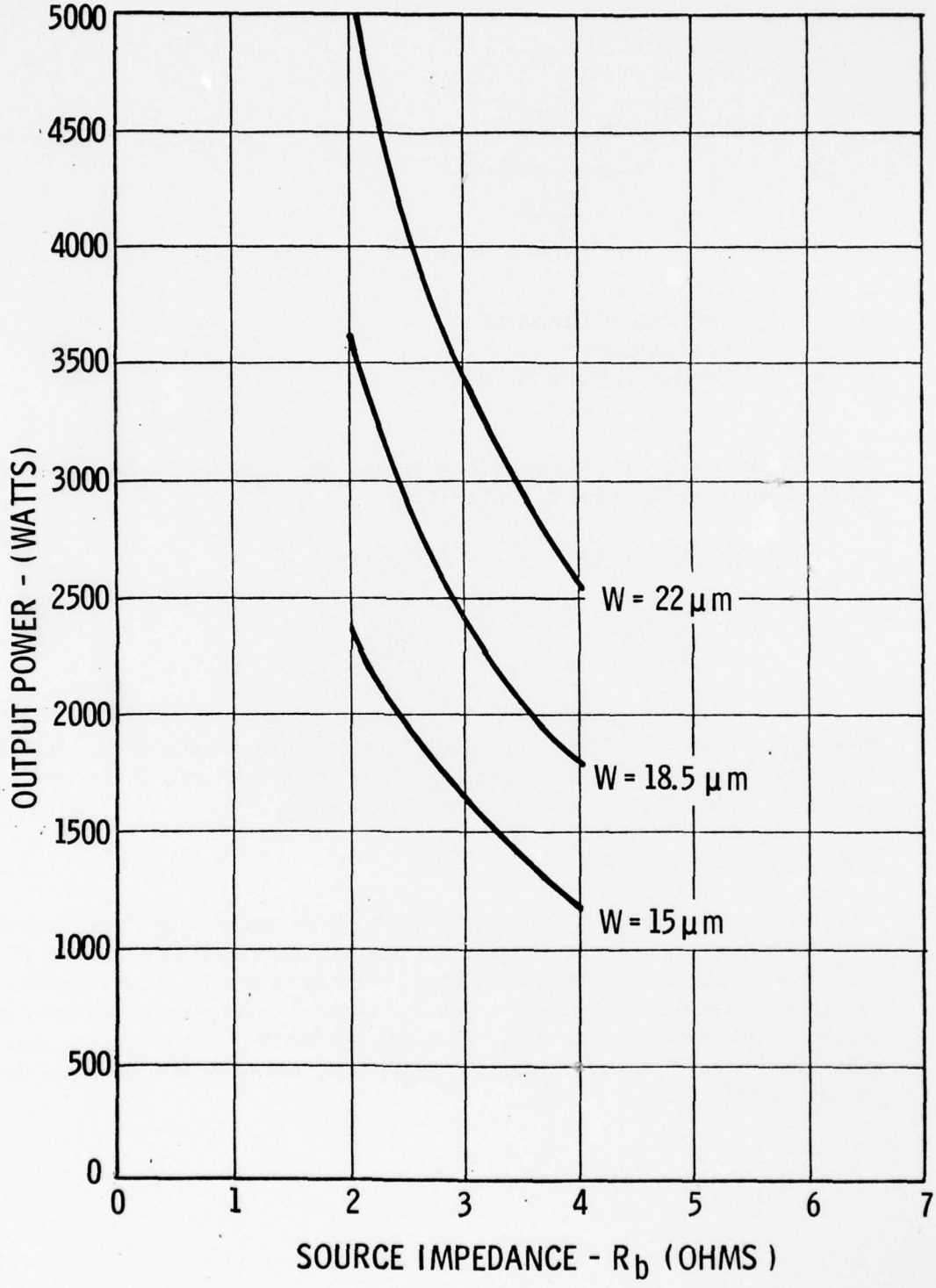

FIG. 2-1 - Peak Diode Output Power vs. Diode Source Impedance

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$$\eta_\pi = \frac{\sin \frac{\pi f \omega}{V_e}}{\frac{\pi f \omega}{V_e}}$$

f	=	frequency of operation
ω	=	epi thickness
v_e	=	electron velocity in silicon

The following table lists the calculated transit-time efficiencies for three epi thicknesses when operated at 1.03 GHz.

Epi Thickness	Efficiency
15 μm	88%
18.5 μm	83%
22 μm	76%

An epi thickness of 18.5 μm was selected; calculations showed that a thicker epi would not result in significantly greater output powers and the overall efficiency would be reduced below acceptable levels.

c. Diode Area and Geometry

The optimum diode area is determined by the diode source impedance and the epi thickness. Fig. 2-2 shows a plot of optimum diode area as a function of these two parameters. For the selected values of the 3 ohm source impedance and 18.5 μm epi thickness, a diode area of 12 mm^2 is required. The diode geometry was chosen to be circular; this geometry results in the maximum beam efficiency because of the circular electron beam, and it results in the minimum excess capacitance.

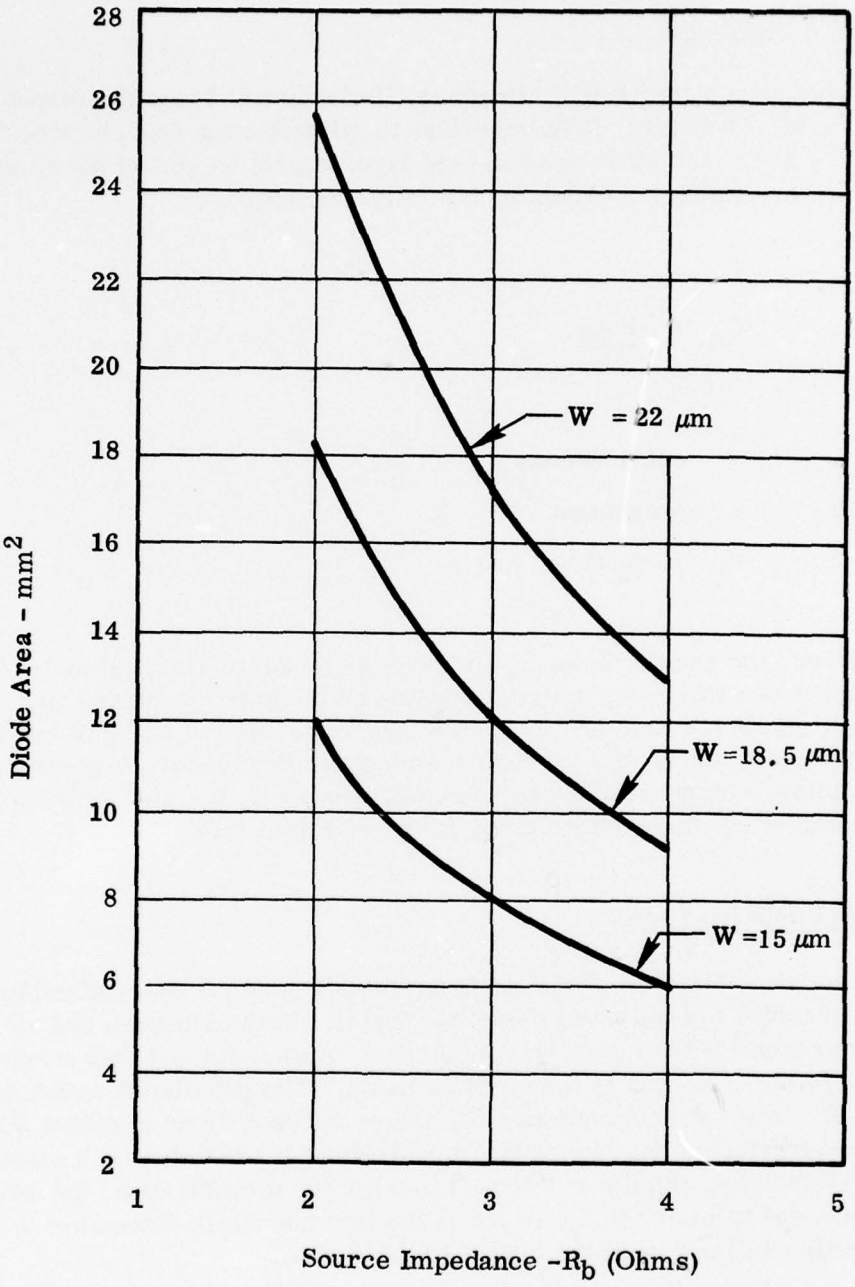

Fig. 3-2. Optimum Diode Area Versus Load Impedance.

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d. Diode Capacitance

The diode capacitance will affect the efficiency and hence the output power of the device; therefore, it is important to minimize the capacitance. The capacitance due to the diode area and epi layer cannot be varied once those parameters are fixed; it is given by the following equation:

$$C_d = \frac{k A_d}{\omega}$$

ω = epi thickness

k = A constant

A_d = diode area

However, the excess diode capacitance due to guard ring and metal overlay capacitance can vary greatly, depending on the diode mask design. Previously measured diodes have shown a total capacitance of 1.3 to 2.0 times the theoretical capacitance, due to this excess capacitance. For design purposes, an excess capacitance factor of 1.5 was selected. However, the goal of the program was to achieve an excess capacitance factor of 1.3 to 1.5.

e. Diode Resistive Losses

The series resistance of the diode top metallization is determined by both the type of metal and the thickness of the metal. Both aluminum and nickel silicide have previously been used on EBS diodes. Aluminum has both a lower resistivity and a lower dead loss to the electron beam. The calculated resistance for a 1000 Å layer of aluminum is .023 ohms; a 200 Å layer of nickel silicide, which has a comparable dead loss, has a resistance of .288 ohms. Because of these considerations, aluminum was selected for the metallization; the extremely low current densities in the diode due to the low duty cycle determine that electromigration will not limit the MTBF of the device.

f. Diode Breakdown Voltage

The diode breakdown voltage is controlled by the epi thickness, epi doping, junction curvature, and the use of a metal field plate above the diode junction periphery. Fig. 2-3 shows the predicted breakdown voltage for 10 ohm-cm material with various epi thicknesses and junction curvatures and no field plate. For the 18.5 μm epi thickness, the maximum breakdown voltage is 260 volts. With the use of a field plate, this could be increased to 320 volts. Some degradation of the breakdown voltage is expected when the diodes are exposed to the electron beam; results with previously developed Watkins-Johnson diodes has shown that this is typically 10 percent.

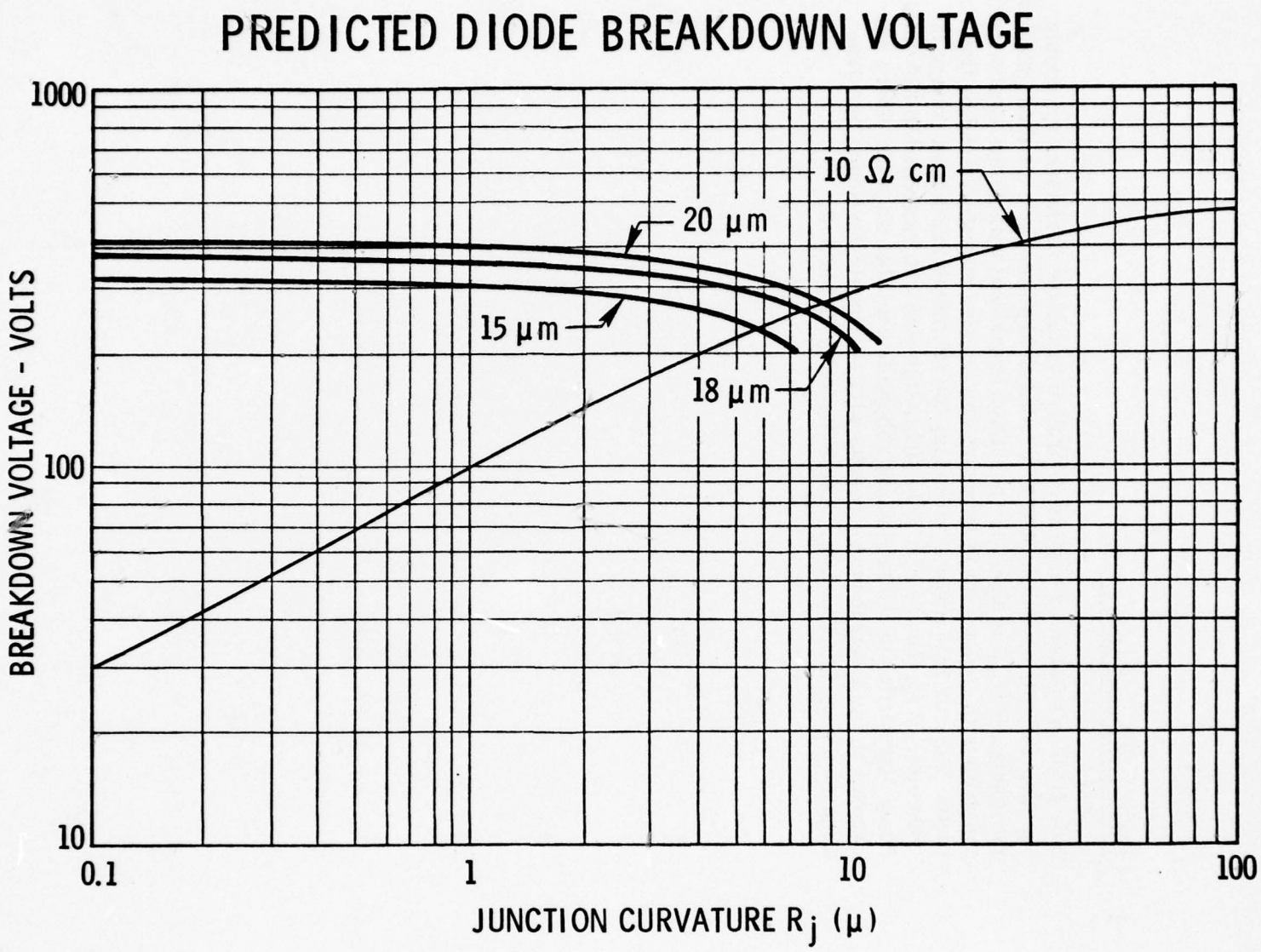


FIG. 2-3 - Predicted Diode Breakdown Voltage

3. DEVICE DESIGN

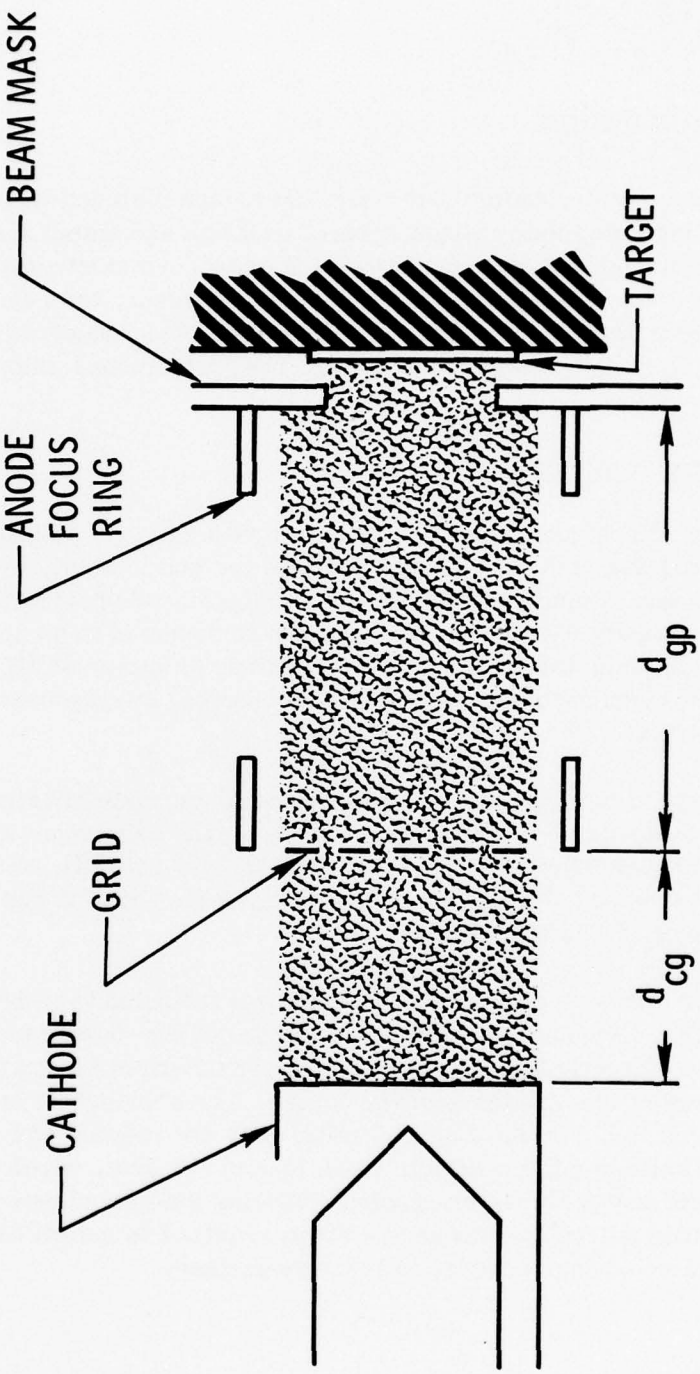
The device mechanical and electrical design included the design of the electron gun, input dc block, target holder, heatsink and output matching circuit. The electron gun was a modification of the standard electron gun design currently in use with other gridded EBS devices; however, the rest of the sub-assemblies required new designs. With the exception of the electron gun, all of these assemblies were fabricated and evaluated for performance prior to incorporation into the device.

a. Electron Gun Design

The electron gun is a triode-type gun with a planar cathode and a close-spaced, intercepting grid. A cross-section of the gun is shown in Fig. 3-1. Focusing of the gun is electrostatic with no separate anode potentials required, simplifying power supply requirements. The gun is designed to be non-convergent; the cathode diameter is 250 mils with a diode diameter of 175 mils, allowing a sufficient overlap to account for any mechanical misalignments between the gun and the target.

Construction of the gun is standard metal-ceramic construction. The design is both inexpensive to fabricate and rugged; the same gun, when used in gridded EBS switches has been tested to MIL-E-5400 and MIL-E-16400 specifications, with an extended temperature range of -54 to +125° C and an extended vibration range of 15 G's to 2000 cps.

For the present application, the gun was modified to reduce the grid-cathode spacing. Because the electron beam is density-modulated by the RF signal applied directly to the grid-cathode, transit-time losses through this region will affect the efficiency of the device. The standard 12 mil cold spacing was reduced to a cold spacing of 7 mils, or a hot spacing of 5 mils. This spacing was limited by the available mesh size of the grid, which was 1 mil mesh with a 6 mil center to center spacing. Moving the grid closer to the cathode would result in a greatly increased voltage required to cut off the electron beam, with a resulting decrease in transconductance.


BEAM MASK
TARGET
ANODE
FOCUS
RING
GRID
CATHODE
d_{gp}
d_{cg}

b. DC Block Design

Two types of DC blocks were developed and fabricated for this program. The DC block is used for isolating the input RF signal at ground from the electron gun potential of 10 to 12.5 kV. The DC blocks are shown in Fig. 3-2. The top DC block is an extremely broadband block designed for laboratory use. It has a -1 dB bandwidth of 300 to 1600 MHz with an isolation of 14 kV. Fig. 3-3 shows a plot of measured loss versus frequency. The second DC block is a low cost, narrow-band DC block which can be designed for any 100 MHz band from 500 to 1500 MHz. It provides an isolation of greater than 20 kV and can be produced for a cost of less than $5, excluding connectors.

c. Target Holder/Output Window Assembly

The target holder/output window assembly provides the mechanical mounting for the diode and beam mask, heat sinking for the diode, and the vacuum window for coupling out the RF signal. A cross-section of the assembly is shown in Fig. 3-4. The diode is brazed to a moly substrate which, in turn, is brazed to the center conductor of the window. The moly substrate is required as a mechanical interface between the silicon diode and the copper; it was found during die-attach tests that due to the difference in thermal expansion rates of silicon and copper, stresses would be placed on the diode as a result of brazing the diode to the copper. Because the thermal expansion rate of moly closely matches silicon, it was chosen as the interface layer. Subsequent tests showed no signs of stress induced after die-attach. The copper center conductor is supported by a BeO window, which is brazed to the heatsink. The BeO was chosen to provide the electrical isolation while providing a low thermal impedance path from the diode.

Because the target holder/output window assembly is at the low impedance (3 ohm) end of the cavity, resistive losses in the assembly could seriously degrade the efficiency. To reduce these losses, the window was designed with as large a diameter as possible to increase the unloaded Q and to reduce contact resistance losses between the window and the cavity. In addition, the BeO window was experimentally optimized to provide the minimum electrical loss while providing a low thermal impedance path. Three different BeO window designs were evaluated.

The first design, window #1, utilized a flat BeO ceramic disc to provide a compromise between thermal and RF losses. Window #2 provided a very good thermal path with a larger volume of ceramic. Window #3 utilized a very low volume of ceramic to minimize RF losses at the sacrifice of some thermal impedance. To compare the designs, the RF losses were measured with the network analyzer.

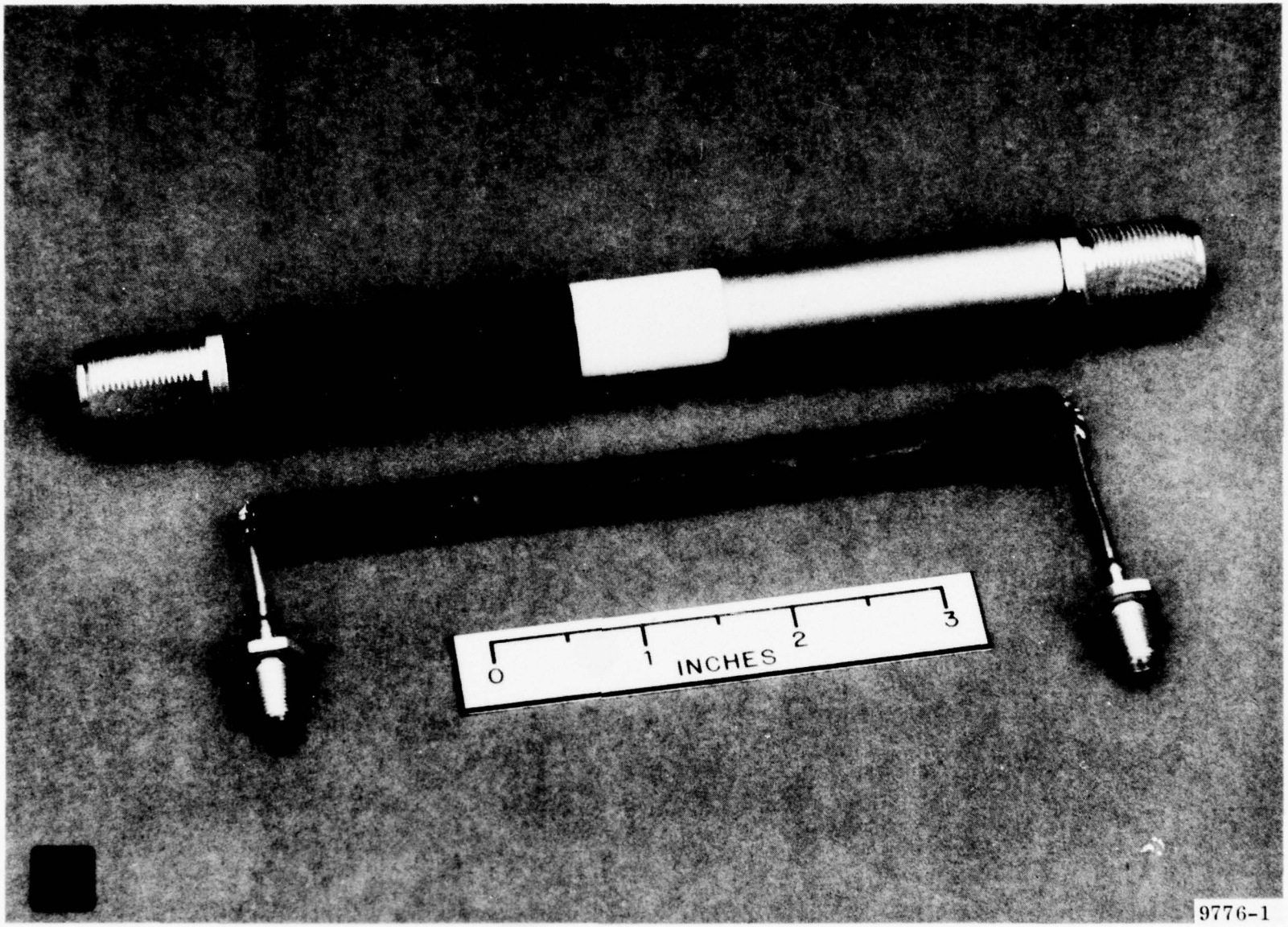


FIG. 3.2 - DC Blocks for RF Transmission

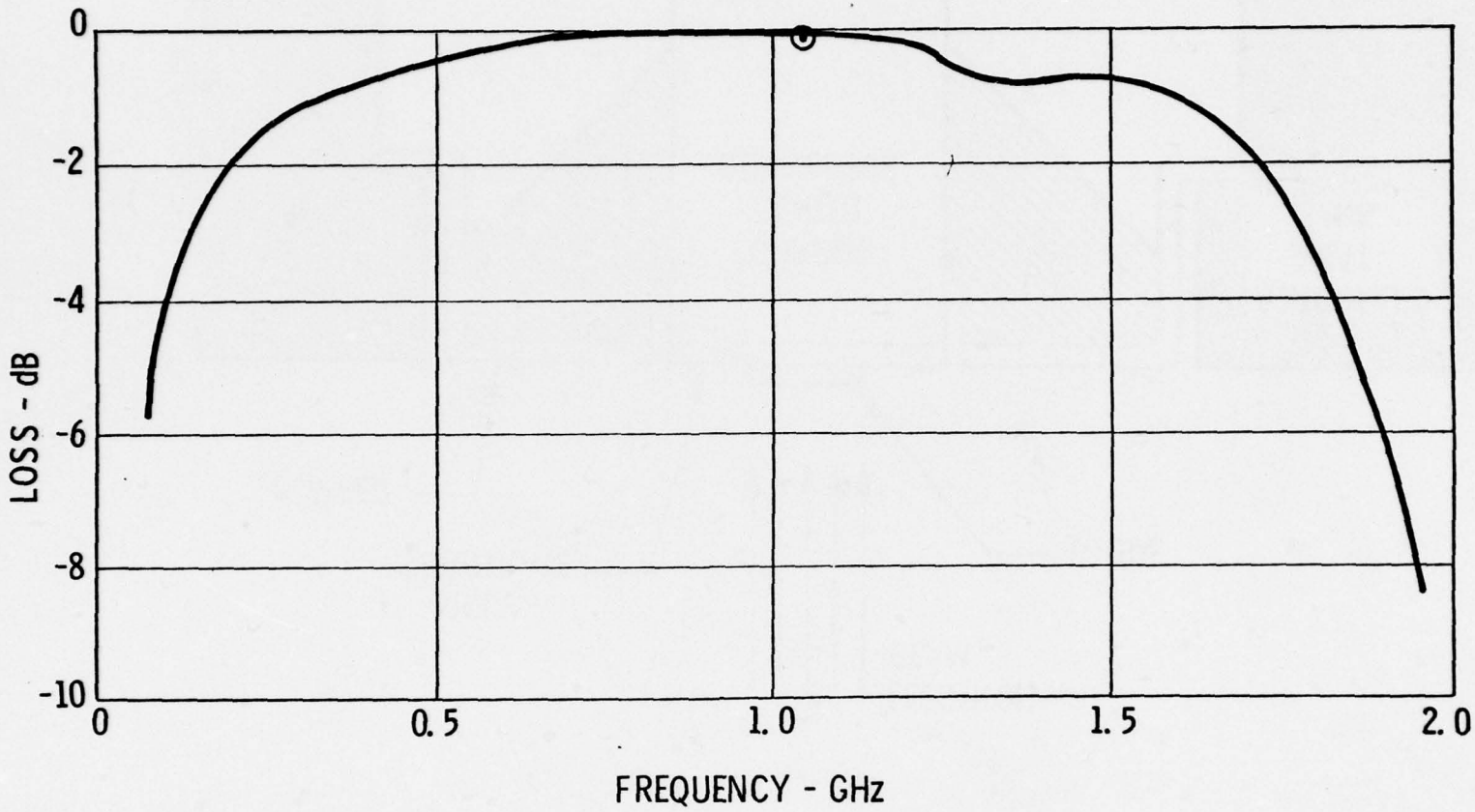


FIG. 3.3 - Loss vs. Frequency of DC Block

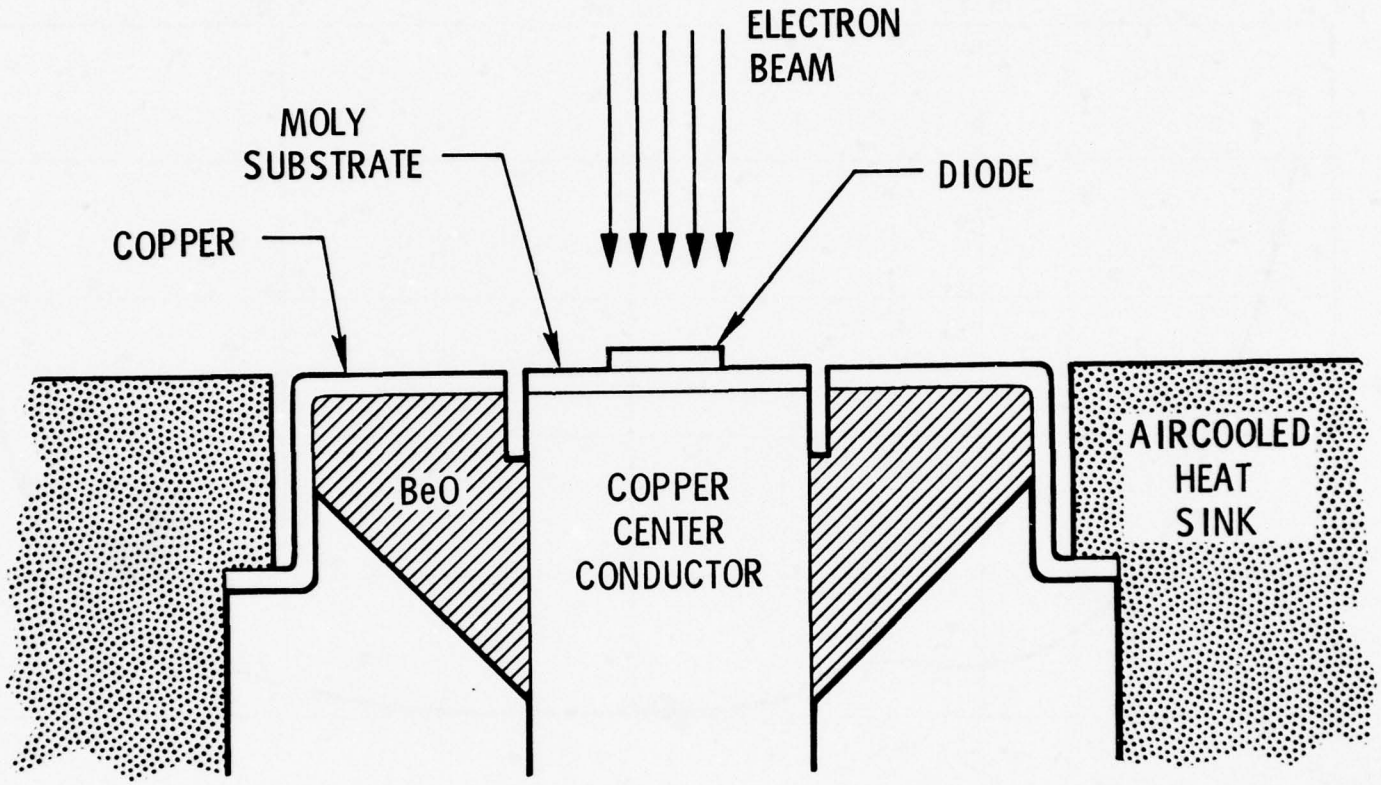


FIG. 3.4 - Cross-section of Target Holder/Output Window Assembly

Wire bonds were used to form a short circuit in place of the EBS diode to eliminate the effect of any diode losses. Window #1 was measured first; 109 1.5 mil aluminum wires were used to form the short-circuit. The measured Q was 400 at a center frequency of 975 MHz. The total resistive loss of window #1 is .049 ohms; since this includes the .033 ohm loss of the cavity, the RF loss of .016 ohms through the window and wire bonds is quite low. It was also possible to measure the effect of the number of wire bonds on performance, to determine how many wire bonds are needed on a target. Wires were gradually removed while the effect on the Q and center frequency were measured. Table 3-I summarizes the results. Above 50 wires, there is almost no additional effect on performance. The shift in center frequency is caused by the increased inductance of the target as the number of wire bonds is reduced. The inductance of a single wire bond, calculated from this shift in frequency, is 1.62 nH, which is within five percent of the theoretical inductance for a length of wire of the given diameter.

The second window was measured under the same conditions. The measured Q was 300 at a center frequency of 887 MHz. The lower center frequency is a result of the larger volume of ceramic in the window. The resistive loss in the window and wire bonds was double that of the first window, .032 ohms. However, even these losses were quite low; because of this, it was decided not to test the third window, as both of the first two designs offered lower thermal impedances with excellent RF performance.

d. Output Matching Circuit

The output matching circuit was developed to match the diode into the required 3-ohm source impedance and transform this impedance up to the 50 ohm output impedance. The matching circuit consists of a quarter-wave cavity followed by a variable coupling capacitor. Fig. 3-5 shows a schematic of the circuit and the diode. The coupling capacitor is variable to allow optimization of the circuit while operating, to achieve the maximum output power.

The output matching circuit was designed mechanically to minimize any resistive losses. Fig. 3-6 shows a photograph of the completed cavity, with the near end being the low impedance end. A large diameter BeCu finger contact is used to provide the electrical connection to the center conductor of the window, minimizing losses. At the 50 ohm end of the cavity, an OSM connector is used which connects to the center conductor of the cavity by another BeCu finger contact. To adjust the coupling capacitance, a metal sleeve slides over a gap in the center conductor; by adjusting the position of this sleeve the capacitance can be varied.

TABLE 3-1

EFFECT OF THE NUMBER OF WIRE BONDS
ON UNLOADED Q AND CENTER FREQUENCY

No. of Wire Bonds	Unloaded Q	Center Frequency
1	85	728
2	118	850
4	188	919
6	209	936
8	219	941
10	239	948
12	254	952
15	284	959
20	327	967
25	346	965
32	369	968
42	390	970
52	397	972
62	394	974
75	398	975
90	398	975
109	402	975

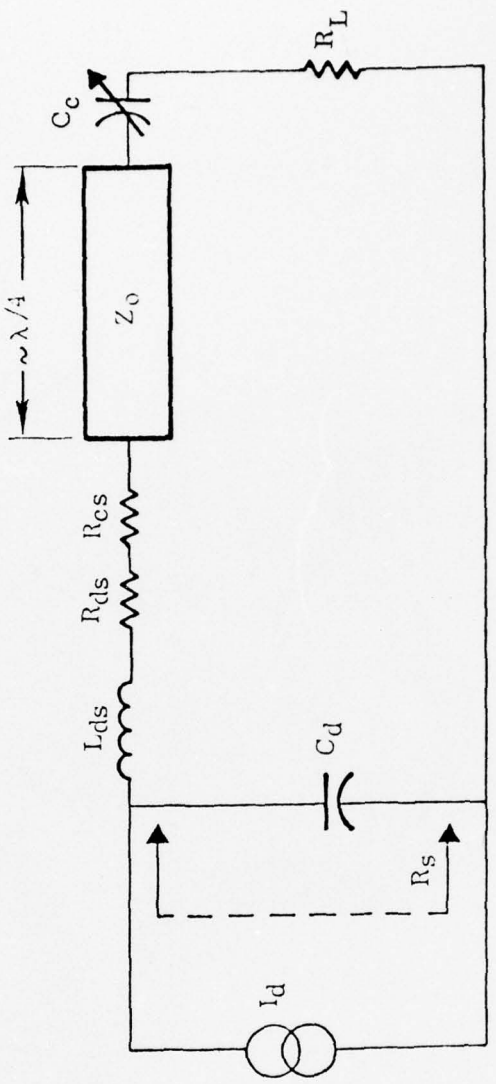


FIG. 3.5 - Schematic of Diode plus Output Matching Circuitry

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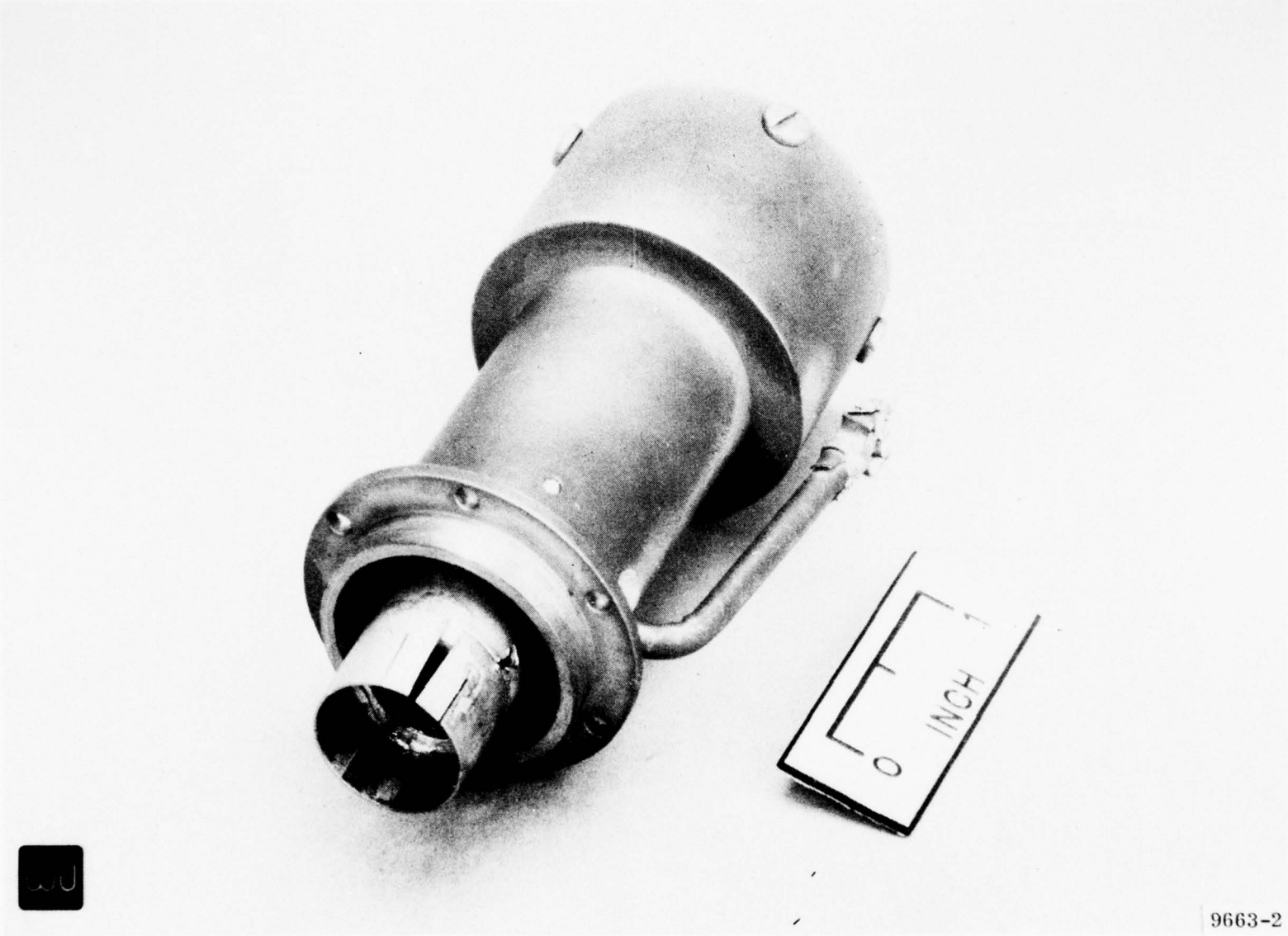

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FIG. 3.6 - Photograph of the Output Cavity

The cavity was measured with a network analyzer to determine the resonant frequency and Q of the cavity. A short was used in place of the output window and target holder, so that only the losses of the cavity would be measured. Under these conditions, the resonant frequency was 1005 MHz and the Q was 1150, representing a resistive loss of .017 ohms. With the addition of the coax-line for biasing of the diode, the Q was reduced to 600, or a total cavity resistive loss of .033 ohms. The low losses show that the BeCu finger contacts are providing a very good RF contact.

4. DIODE FABRICATION

Fabrication of the diodes for this program was performed in the EBS diode facility at Watkins-Johnson Company. The fabrication was similar to previously-developed diodes except that the extremely large area of the diodes combined with the thin, highly doped epi made process control extremely important. Problems were encountered early in the diode fabrication which resulted in low yield, high diode leakage currents and diode failure during operation at normal stress levels. Using in-house and outside analytic methods, the cause of these problems was traced to materials defects in the starting material purchased by Watkins-Johnson and to defects introduced during processing at Watkins-Johnson. These defects were of a small magnitude normally considered acceptable in the semiconductor industry; however, due to the more severe requirements of these diodes, these defects introduced the above-mentioned problems. Elimination of the defects involved new starting material, new processing equipment, and modifications to the diode processing schedule. With these modifications, diodes were fabricated with high yield, low leakage currents, and reliable operating characteristics.

a. Diode Fabrication

A cross-section of the standard EBS diode is shown in Fig. 4-1a. The wafer is started as an 8 mil thick N^+ silicon substrate with a 22 μm, 10 ohm-cm epi layer grown on top. Silicon dioxide is grown over the entire wafer. The silicon dioxide is then removed from the active area and the P^+ guard ring and active area layer are diffused into the epi layer. A passivation layer of phosphorus-doped glass is deposited over the entire wafer and removed from the active area, leaving the passivation layer to protect the junction areas. The thin aluminum and thick aluminum layers are then evaporated on to the wafer. Finally, the wafer backside is ground, polished, and metallized.

Fig. 4-1b shows an alternate method of diode fabrication utilizing a metal field plate to increase the diode breakdown voltage. The diode is fabricated with a much thinner oxide layer over the junction area of the diode. The thick layer of aluminum deposited over the oxide acts as a field plate to limit the peak electric field developed in the junction area, thus increasing the breakdown voltage.

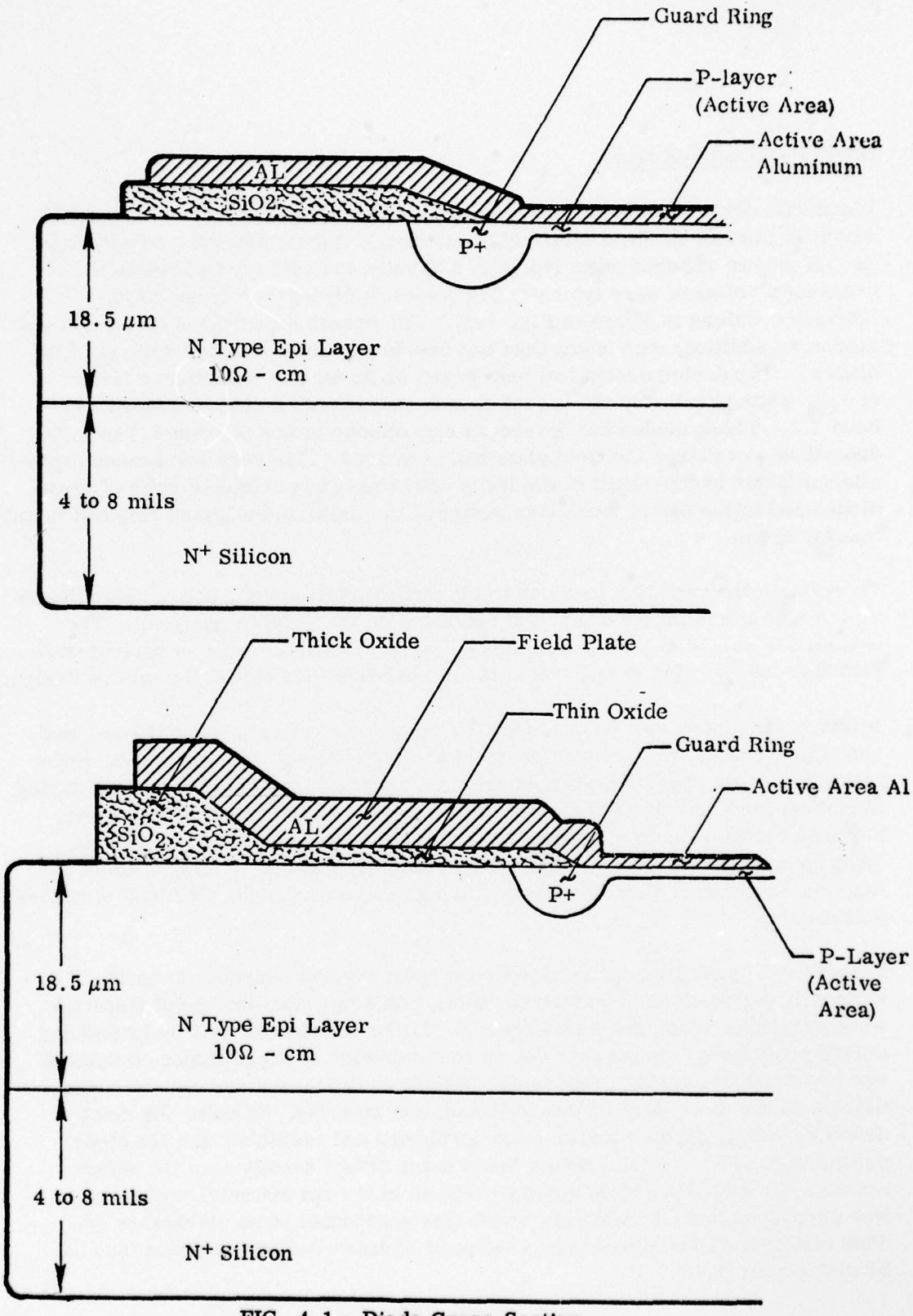

FIG. 4-1 - Diode Cross-Section

b. Diode Fabrication Results

The initial diode fabrication run resulted in diodes with breakdown voltages within 10 percent of the theoretical breakdown voltages; without the field plate the breakdown voltages were typically 230 volts and with the field plate the breakdown voltages were typically 270 volts. A photograph of one of the fabricated wafers is shown in Fig. 4-2. The excess capacitance factor of these diodes, in addition, was lower than had previously been obtained with any EBS diodes. The device design had been based on an excess capacitance factor of 1.5, while previously the lowest excess capacitance factor measured had been 1.3. These diodes had an excess capacitance factor of from 1.1 to 1.2, depending on whether the field plate had been used. This very low excess capacitance factor is the result of the large active area to perimeter ratio of these diodes and to the use of mask sets designed to minimize the guard ring and metal overlay areas.

To evaluate the resistive loss due to the diode metallization, one of these diodes was brazed into a target mount and evaluated on the network analyzer. The unloaded Q was 166 with a center frequency of 970 MHz. This is equivalent to a resistive loss of .111 ohms, which is the resistive loss calculated for the design.

Although the diodes met or exceeded the breakdown voltage, capacitance, and resistance goals, they showed low yield and high leakage currents. The diode leakage current would increase during high temperature processing, both during aluminum alloy and device bakeout. In addition, the diodes would fail under normal operating conditions when on test. The symptoms indicated that the failures and high leakage currents were caused by defects or impurities in the material introduced either before or during processing of the diodes at Watkins-Johnson.

Defects and impurities can be introduced from several sources. Defects, primarily dislocations and stacking faults, can be present in the epi material when purchased from an outside source. These defects can also be introduced during processing. Impurities due to contamination of the diffusion equipment can be introduced during processing. Defects in the masks can also introduce defects on the diode surface due to incomplete masking. To solve the mask defect problem, chrome masks were purchased and instituted into the diode processing. These masks have a much lower defect density than the standard masks. To solve the defect density problem in the epi material, epi material was purchased from Semimetals which was guaranteed to be dislocation free. This material was analyzed upon receipt at Watkins-Johnson and was found to be dislocation free.

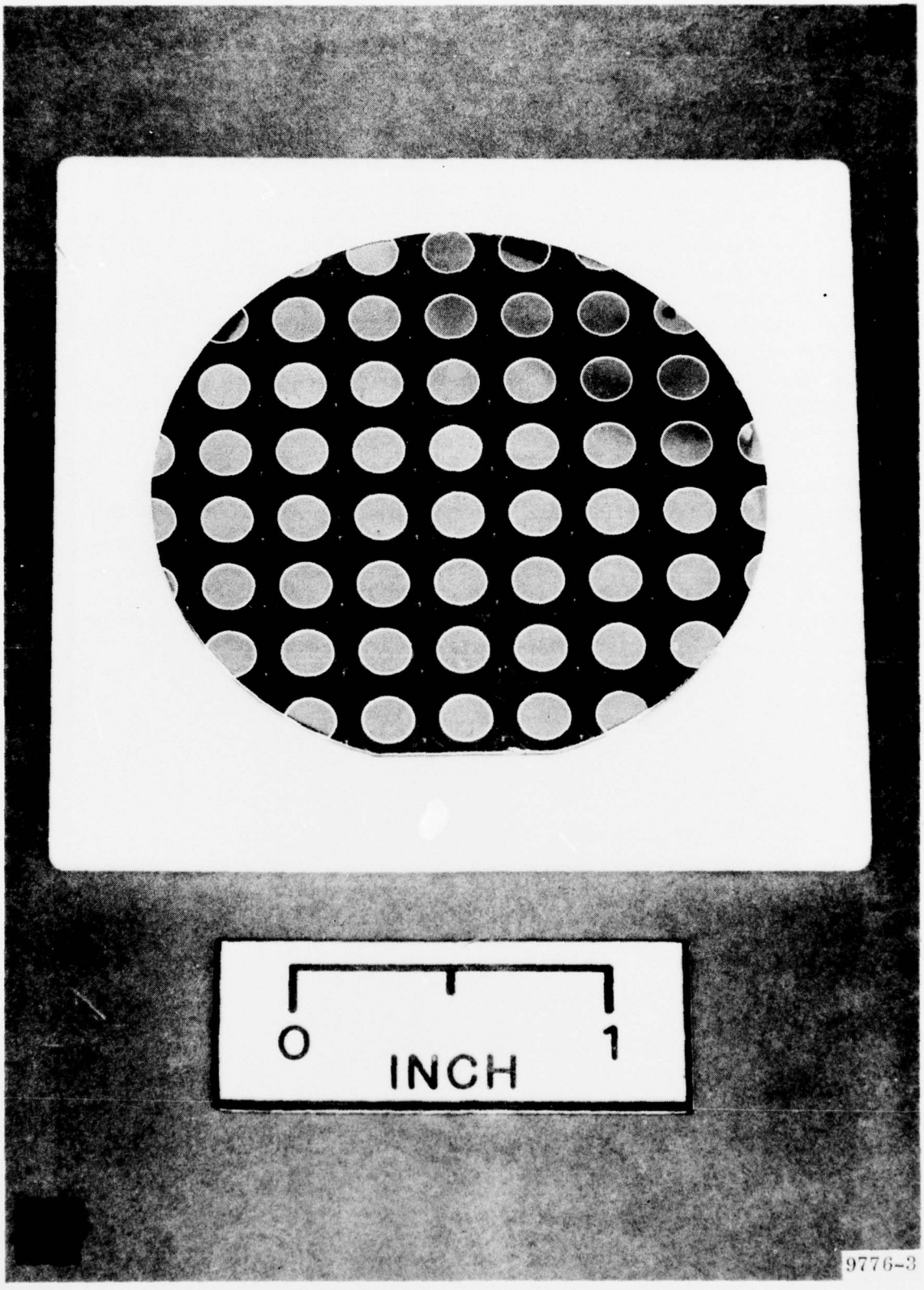

FIG. 4.2 - Photograph of completed wafer.

The elimination of any defects or impurities introduced during the diode processing is typically quite difficult because of the extremely high temperature cycles that are required. One possible solution that had been discussed in the literature was the use of some type of controlled impurity introduced into the back side of the wafer to getter out impurities. Several types of getters were investigated at Watkins-Johnson; SiP207 was found to give the best results. In addition, the quartz boats and furnace tubes which are typically used in the semiconductor industry were replaced with silicon boats and furnace tubes. The silicon is considerably more expensive than the quartz but is also much purer. Since these boats and furnace tubes are used during the high temperature diffusions, any impurities released from the quartz could diffuse into the silicon wafer.

With the incorporation of the chrome masks, dislocation free epi, silicon processing equipment, and gettering, two diode runs were fabricated. Both of the runs produced a high yield of diodes with extremely low leakage currents. Fig. 4-3 shows the I-V characteristic of one of these diodes. At breakdown, the leakage current is much less than 1 μA. The diodes were processed through aluminum alloy and device bakeout with absolutely no change in the diode leakage current. No failures have been encountered with these diodes on test, and the diodes have shown no degradation in their I-V characteristics during operation.

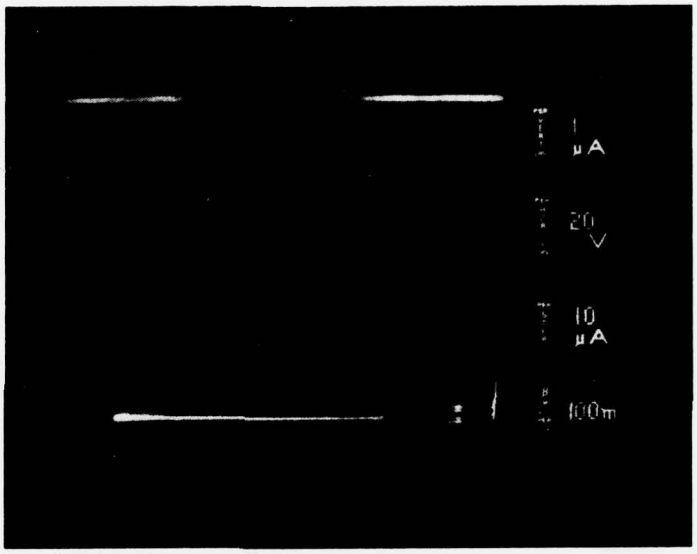

FIG. 4.3 - Diode I-V Characteristic

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5. DEVICE TESTING AND PERFORMANCE RESULTS

a. Burn-in Procedure

During the program a total of seventeen devices were fabricated and tested. The devices, once assembled, were placed on bakeout at 250°C with a 110L/sec vacuum pump pulling the vacuum. The bakeout was continued for a minimum of 50 hours, with the dispenser cathode activated during this period. After the device was pinched off from the main vacuum pump, a 2L/sec pump was used to continue pulling the vacuum. The device was next operated with the electron beam striking the diode, which was not biased. This stabilized the cathode emission and continued outgassing of the device. However, during the program it was discovered that this outgassing procedure was damaging the diodes, as a substantial amount of power was being dissipated in the diode even with no bias voltage applied. This was remedied by outgassing the device with the N side of the diode open-circuited so that there could be no current path through the diode. Once the device was sufficiently outgassed, the 2L/sec pump was pinched off, leaving the device ready for testing (It was possible to test the devices with the pump attached, but this increased the risk of oscillation). Figure 5.1 shows a photograph of one of the pinched-off units with the cavity attached, ready for testing.

b. Oscillation Suppression

Because of the extremely high gain of the EBS L-Band amplifier, the device is susceptible to oscillation caused by coupling between the input and the output. This oscillation can cause device failure by causing the device to go CW and exceed the power dissipation limits of the diode. Two types of coupling can cause the oscillation; internal capacitive coupling between the target and the grid, and external coupling between input and output circuitry. To eliminate the internal coupling, the devices were operated common grid, i.e. the grid was the common element at high voltage and the RF signal was applied to the cathode. The grid then acts as a shield, virtually eliminating coupling between the cathode and the target. To shield from external coupling, the input DC leads (heater and cathode) were run through RFI filters and the gun end of the device was encased in a shielded box. In addition, the diode bias lead was run through an RFI filter. Using these shielding techniques, the devices showed no tendency to oscillate over the entire operating range.

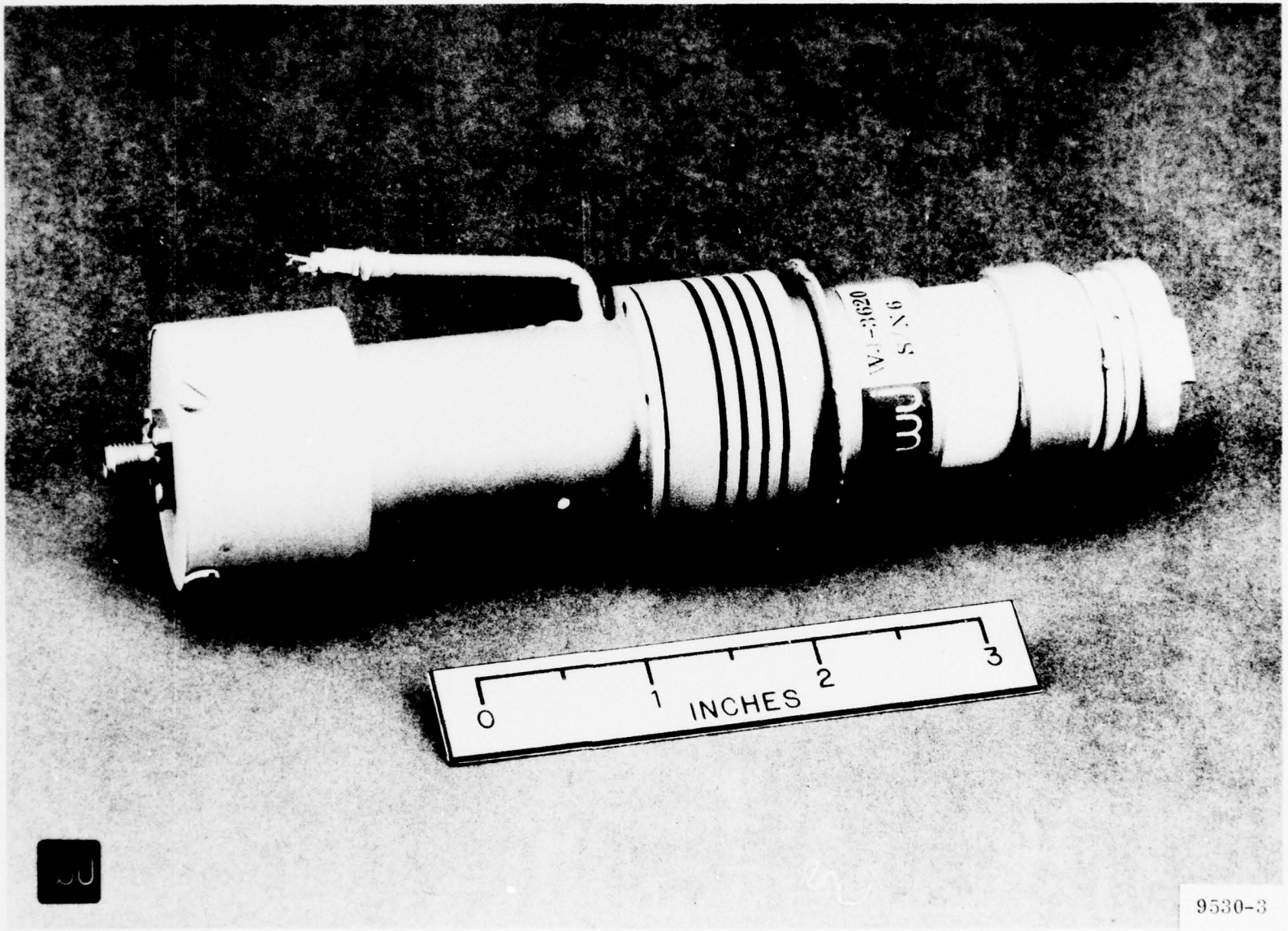

FIG. 5.1 - Pinched-off Device with Output Matching Cavity

c. Power Supply Hook-Up

Figure 5-2 shows a schematic of the power supply hook-up. Four supplies are required; the heater supply, grid bias supply, beam supply, and diode bias supply. Since the electron beam acts only as a control element, the beam supply requires very little power, in this case 2.4W or about 10% of the diode bias supply power. The device also requires no separate pulser for modulating the RF; the device is normally biased off with the grid bias supply; the RF input can be modulated at ground with the RF swing turning the device on.

d. Test Results

Utilizing the diodes fabricated during the early part of the program, devices were tested with up to 700W peak output power and typical efficiencies of 38% at 1GHz and 50% at 500MHz. It was possible to demonstrate the thermal dissipation capabilities of the design; one device was operated under DC characteristics with 45W of power dissipation; a second device was operated with 16W of average RF output power and 30W of power dissipation.

With the diodes fabricated in the last diode fabrication runs which showed the lack of defects, two devices were fabricated and tested. The first of these was tested to 1150W peak output power. It showed no signs of degradation during bakeout or testing. The measured transfer curve for this device is shown in Figure 5-3. The second device was tested to 1000W at 1% duty cycle and operated at that level for 60 hours with no signs of degradation. The device was operated to peak output powers of up to 1500W. This device also was extremely stable during testing and showed no signs of diode degradation during operation. The measured bandwidth curve is shown in Figure 5-4.

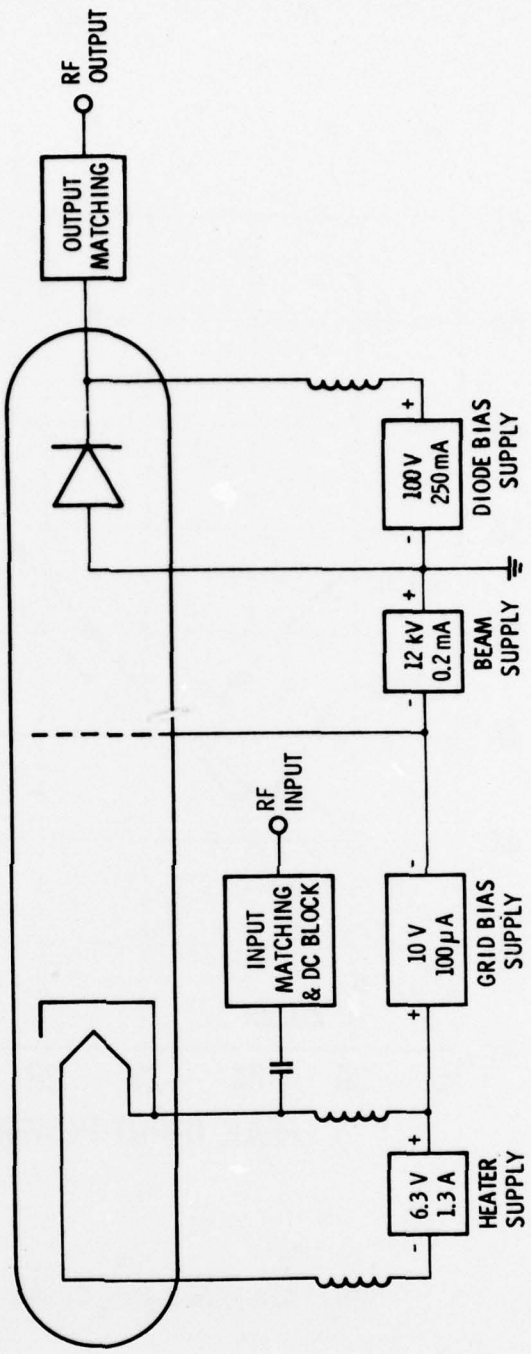

FIG. 5.2 - Power Supply Schematic

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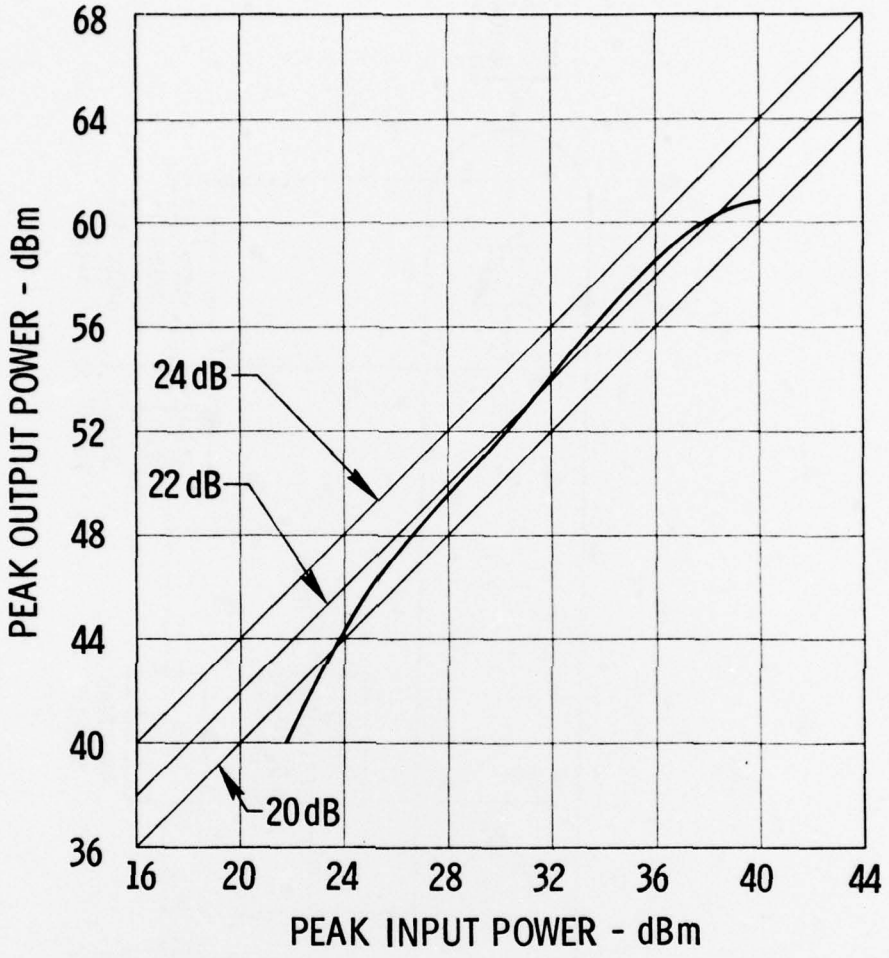

FIG. 5.3 - Transfer Curve

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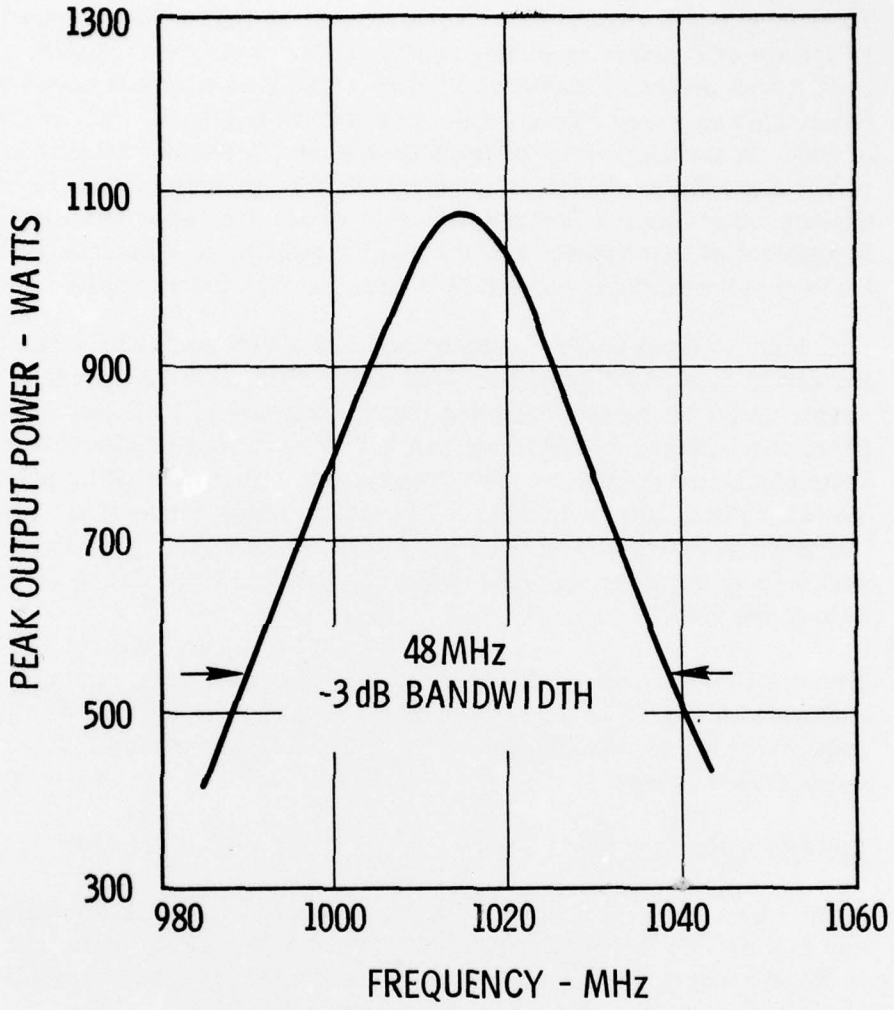

FIG. 5.4 - Bandwidth Curve

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6. CONCLUSIONS AND RECOMMENDATIONS FOR FURTHER WORK

This program has led to the development of an EBS L-Band amplifier uniquely suited for IFF power amplifier applications. The device has demonstrated a peak output power of 1000W at 1% duty, 1500W peak output power at 0.1% duty, power gain of greater than 23dB, a bandwidth of 50mHz, and a target efficiency of 50%. In addition to the performance goals, a number of significant achievements were made on this program which have greatly increased the state-of-the-art capability for EBS amplifiers. These are listed in table 6-I. The most significant of these achievements if the capability to fabricate reliable, low-leakage current, large area EBS diodes for high power applications such as this.

The demonstrated performance levels of the EBS amplifier make it highly attractive for use in Army IFF systems. Use of the EBS can be expected to improve system performance by greatly reducing transmitter power variation with life. In addition, the EBS has demonstrated an MTTF in excess of 150,000 hours in life tests conducted during the past three years. Thus, it will be possible to reduce overall system life cycle costs by reducing maintenance of the power amplifier. Further improvements in reliability, and reductions in procurement cost, will result from the elimination of numerous driver stages due to the extremely high gain of the EBS.

Present EBS L-band amplifiers have demonstrated the output power and gain required for use in IFF Transponders. Even so, additional development is required prior to introduction of the EBS in Army systems. These tasks are summarized below:

Electrical Performance:

Additional electrical development is required to increase amplifier efficiency and to increase the design margins for output power and gain. Improvements in these areas will contribute to reduced system power consumption, improved overall reliability and reduced amplifier cost.

The diode efficiency (ratio of RF output power to diode bias power) is currently 34-38 percent for EBS amplifiers at 1 GHz. This results in an overall amplifier efficiency of approximately 25-28 percent. In contrast, EBS UHF amplifiers have recently demonstrated diode efficiencies of over 60 percent and overall efficiencies in excess of 50 percent. Improvements in the design of the semiconductor diode can be expected to produce similar increases in EBS L-band amplifier efficiency.

TABLE 6-I

SIGNIFICANT ACHIEVEMENTS

MECHANICAL

- RUGGED, PRODUCTIZED DESIGN
- SUBSTANTIALLY REDUCED COST OF DEVELOPMENT DEVICES
- LOWERED THERMAL IMPEDANCE OF OUTPUT WINDOW

OUTPUT CIRCUIT

- SIGNIFICANTLY REDUCED OUTPUT CIRCUIT LOSSES
- DEVELOPED CAVITY WITH WIDE ADJUSTMENT RANGE
- DEVELOPED BOTH 500 MHz and 1 GHz CAVITIES

INPUT CIRCUIT

- DEVELOPED BROAD BANDWIDTH DC BLOCK
- DEMONSTRATED RF MODULATION AT GROUND
- DEMONSTRATED 23 dB POWER GAIN

ANALYTIC DESIGN & EVALUATION

- OPTIMIZED DIODE SOURCE IMPEDANCE
- OPTIMIZED DIODE AREA, MATERIAL THICKNESS, & DOPING

SEMICONDUCTOR TARGET

- RELIABLE AND LOW THERMAL IMPEDANCE DIE ATTACH
- FABRICATED LOWEST LEAKAGE CURRENT LARGE AREA DIODES
- ACHIEVED LOWEST EXCESS CAPACITANCE

PROCESSING

- EIGHT DIODE RUNS FABRICATED
- PHOSPHORUS GETTERING
- WAFER THICKNESS DOWN TO 4 MILS

A goal of 50 percent overall efficiency appears practical. Increased amplifier efficiency provides multiple benefits. Increased efficiency reduces system prime power consumption. Reduced power consumption permits use of less expensive power supplies which contributes to a significant reduction in overall amplifier cost. Furthermore, increased efficiency allows the use of less expensive mechanical designs due to less critical thermal impedance requirements.

Improvements are also required in the electron gun in two areas. The grid-cathode transit time of the present gun is excessive, contributing to reduced amplifier efficiency. Transit time can be reduced through a decrease in grid-cathode spacing which will also require a reduction in grid mesh size. Furthermore, construction of the present grid-cathode support results in excess input capacitance which reduces the available amplifier gain and requires a high Q input match. Reduction of grid-cathode capacitance will provide higher amplifier gain. Of even more importance, reduced input capacitance will provide a low Q input match, allowing the use of simple, inexpensive and non-critical input matching techniques. Thus, improvements in the electron gun can be expected to contribute to improved efficiency and gain and will result in an amplifier design which can be produced at lower cost.

A final area which should be stressed in improving electrical capabilities is the performance margin provided in critical areas such as output power and gain. It is a widespread experience with electronic components that the provision of adequate performance margins plays a dominant role in achieving cost and reliability goals. EBS capabilities in critical areas, specifically peak and average power and gain, should be increased to insure that high yield (and hence low cost) and high reliability will be obtained in systems using the EBS.

Integration:

Development of an integrated amplifier consisting of both the EBS and the required power supplies should be initiated. The EBS L-band amplifier has been designed for a simple power supply configuration. For example, RF modulation of the high power output signal is accomplished by simply modulating the low level input signal, thus eliminating the need for any pulsed circuitry within the supplies. Despite the inherent simplicity of the supplies, careful design will be required to insure that adequate EBS and power supply interface protection is provided to insure high reliability while minimizing overall amplifier cost. Development of an integrated EBS amplifier compatible with the buss voltages and RF levels available in Army systems will allow simple retrofit installation of this amplifier in existing systems which now suffer from reliability problems. This amplifier will also form

a basic building block for use in new systems.

Cost Reduction Engineering:

The type construction used in the EBS amplifier was specifically selected because it was compatible with low manufacturing cost. However, the present device has not been designed for minimum cost. It is recommended that a cost reduction engineering development phase be scheduled to precede or coincide with large scale system procurement of the EBS amplifier. It is anticipated that a manufacturing technology program of this type will provide an extremely high cost savings to the Army, compared to the actual program cost. Furthermore, a program of this type would not only dramatically impact the cost of EBS L-Band amplifiers, but would also affect the manufacturing costs for many similar EBS devices using the same fabrication technology such as video amplifiers, switches and UHF amplifiers.